IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Shannon V. Davidson, et al.
Serial No.:	10/825,021
Filing Date:	April 15, 2004
Group Art Unit:	2191
Confirmation No.:	7500
Examiner:	Ted T. Vo
Title:	*System and Method for Topology-Aware Job Scheduling and Backfilling in an HPC Environment*

MAIL STOP: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pre-Appeal Brief Request for Review

This Pre-Appeal Brief Request for Review and the accompanying Notice of Appeal are submitted pursuant to provisions set forth in the Official Gazette Notice of July 12, 2005. Applicants respectfully request reconsideration and allowance of the rejected claims.

Remarks

Claims 1-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hovestadt and Keller et al., *Scheduling in HPC Resource Management Systems: Queuing vs. Planning*, Proceedings of the 9th Workshop on Job Scheduling Strategies for Parallel Processing, Seattle, WA, pp. 1-19, 2003 ("*Keller1*"), in view of Keller et al., *Anatomy of a Resource Management System for HPC Clusters*, Vol. 3, 2001 ("*Keller2*"), and in view of Cisco Systems, *Cisco 12012 Gigabit Switch Router Switch Fabric Cards Replacement Instructions* ("*Replacement Instructions*"). Applicants respectfully submit that the rejections are legally and/or factually deficient and should be reversed.

I. The Combination Fails to Disclose, Teach, or Suggest all Claim Limitations

The cited combination fails to disclose, teach, or suggest each and every limitation of Applicants' claims. Claim 1, which Applicants discuss as an example, recites the following:

> A method comprising:
> determining, using one or more computers, an original subset of a plurality of nodes, the original subset comprising nodes currently unallocated to a job, each node in the plurality of nodes comprising a switching fabric integrated to a card and at least two processors integrated to the card, the

switching fabric allowing node to node communication during execution of a job;

selecting a job from a job queue; and

executing the selected job using one or more processors of one or more nodes of the original subset.

At a minimum, the rejection continues to err both legally and factually by apparently ignoring claim language specifying that each node in the plurality of nodes comprising a switching fabric integrated to a card and at least two processors integrated to the same card, the switching fabric allowing node to node communication during execution of a job.

The rejection acknowledges that *Keller1* does not disclose nodes that comprise a switching fabric integrated to a card and at least two processors integrated to the card. *Final Office Action* at 7. However, the rejection states that "Keller2 shows in a HPC the nodes (in Figure 12) which are hardware-executable elements, comprising a switch to allow the elements [to be] selectable and commutable." *Id.* at 8. The rejection also states that "*Keller2 shows nodes [that] are in Cluster comprising Ethernet Switch* (See Keller2: Figure 13, p. 16)." *Id.* at 7 (emphasis in original). The rejection acknowledges that *Keller1* and *Keller2* "do not mention the 'switches' or cards as of '*switching fabric.*'" *Id.* (emphasis in original). However, the rejection alleges that "Cisco Systems shows switch fabric, switch fabric card, used as the endpoints of Route processors (RP), where a RP executes a job received from such a switch via a scheduler." *Id.*

First, Figure 12 of *Keller2* does not appear to include any depiction of a switch. Figure 13 of *Keller2* merely shows a single switch -- an Ethernet switch. Even assuming for the sake of argument that this Ethernet switch could be considered "a switching fabric" as recited in Claim 1, *Keller2* still would fail to disclose "**each node in the plurality of nodes comprising**" the Ethernet switch. Instead, in *Keller2* the Ethernet switch is completely separate from the two frontend computers and from the 32 compute nodes, which tends to teach away from the arrangement recited in Claim 1. *Keller2*, p. 20. Moreover, even assuming again for the sake of argument that the Ethernet switch could properly be considered "a switching fabric" as recited in Claim 1, *Keller2* still would not disclose that the Ethernet switch is "**integrated to a card**," there being "**at least two processors integrated to**" the same card. Thus, *Keller1* and *Keller2* fail to disclose "each node in the plurality of nodes comprising a switching fabric integrated to a card and at least two processors integrated to the card," as recited in Claim 1.

Second, the cited *Replacement Instructions* describe replacement instructions for a particular model switch router. The cited portions describe a switch fabric as circuitry that carries user traffic between line cards or between the route processor and a line card, and that the switch fabric card contains only the switch fabric circuitry that carries user traffic between line cards or between the RP and the line cards. *See* page 3. Figure 5 shows where the switch fabric card may be installed in the lower cage of the switch router. *See* page 10. While the cited portions use the term "switch fabric" and "switch fabric card," they do not appear to disclose that "each node in the plurality of nodes compris[es] a switching fabric integrated to a card and at least two processors integrated to the card," as recited in Claim 1.

The rejection seems to use the *Replacement Instructions* to allege that the term "Ethernet Switch" in *Keller2* could be considered a "switch fabric." *See Final Office Action* at 5. However, replacing the Ethernet switch of *Keller2* with the switch fabric card of the *Replacement Instructions* (or assuming that the Ethernet switch of *Keller2* is a switch fabric) still would result in a system in which the switch fabric card is completely separate from the two frontend computers and from the 32 compute nodes, which is different than the arrangement of Claim 1. *See Keller2* at 20. Moreover, such a modification still would fail to disclose that the Ethernet switch is "**integrated to a card**," there being "**at least two processors integrated to**" the same card. Therefore, the *Keller1-Keller2* combination, even when modified in the proposed manner using the *Replacement Instructions*, still would fail to disclose, teach, or suggest "determining, using one or more computers, an original subset of a plurality of nodes, the original subset comprising nodes currently unallocated to a job, each node in the plurality of nodes comprising a switching fabric integrated to a card and at least two processors integrated to the card" as recited in Claim 1.

The rejections still have not identified anything in the references allegedly disclosing that each node in the plurality of nodes comprises a switching fabric integrated to a card and at least two processors integrated to the same card. Indeed, it appears that the rejection ignores claim limitations requiring that "each node in the plurality of nodes compris[es] a switching fabric integrated to a card and at least two processors integrated to the card, the switching fabric allowing node to node communication during execution of a job."

As another example of the deficiencies of the proposed combination, the cited portions fail to disclose "determining, using one or more computers, an original subset of a plurality of nodes, the original subset comprising nodes currently unallocated to a job," as recited in Claim 1. The rejection states that "Keller1 shows nodes as hardware resources,"

that the "nodes are used in scheduling for job assignment in HPC systems," and that "some of the nodes are N nodes are unallocated." *Final Office Action* at 3. The rejection cites the "system wide node limit" definition on page 15 of *Keller1*. This node limit is set by an administrator and consists "of a threshold (T), a number of nodes (N), and a time slot [start, stop]." *Keller1* at §4.3. "N defines the number of nodes which are not allocatable if a user requests more than T nodes during the interval [start, stop]." *Id.* A variable set by an administrator and defining a number of nodes that are not allocatable (according to conditions disclosed in *Keller1*) is not the same as an explicit determination, using one or more computers, of a plurality of nodes, the determined original subset comprising nodes currently unallocated to a job, as recited in Claim 1. Furthermore, neither the cited references nor their combination discloses making any such determination with reference to the types of nodes recited in Claim 1. In particular, Claim 1 recites that the determined original subset comprises nodes currently unallocated to a job, that each node in the plurality of nodes comprises a switching fabric integrated to a card and at least two processors integrated to the card, and that the switching fabric allows node to node communication during execution of a job.

Somewhat indicative of the examination of this Application, the rejection: (1) refers to claim language as "generic;" (2) refers to the claims as "broad and being attempted of including the claimed languages that are not straightforward;" and (3) alleges that Applicants' arguments do not comply with 37 C.F.R. § 1.111(b), accusing Applicants of merely making "a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." *Final Office Action* at 4-6. First, while Applicants appreciate a broad interpretation of the claims, the USPTO still must consider each and every limitation recited in the claims when evaluating those claims in light of alleged prior art. As discussed above, the rejection apparently ignores certain claim language. Second, none of the claims is currently subject to any rejections under 35 U.S.C. § 112. Indeed, certain language was previously rejected under such grounds, but those rejections were withdrawn. Third, far from a general allegation that the claims define a patentable invention, Applicants identified particular claim limitations not disclosed in the cited portions of the references and explained how the cited portions of those references fail to disclose those identified claim limitations. Applicants submit that this is a well-accepted, thorough, and appropriate technique for responding to rejections.

For at least these reasons, Applicants respectfully request reconsideration and allowance of independent Claim 1 and its dependent claims.

Independent Claim 9, directed to software, recites that "each node in the plurality of nodes compris[es] a switching fabric integrated to a card and at least two processors integrated to the card, the switching fabric allowing node to node communication during execution of a job." Independent Claim 17 is directed to a system that comprises "a plurality of nodes, each node comprising a switching fabric integrated to a card and at least two processors integrated to the card, the switching fabric allowing node to node communication during execution of a job." For at least certain reasons analogous to those discussed above with respect to Claim 1, the *Keller1-Keller2-Replacement Instructions* combination also fails to disclose, teach, or suggest these limitations recited in Claims 9 and 17, and respectfully request reconsideration and allowance of these claims and their dependent claims.

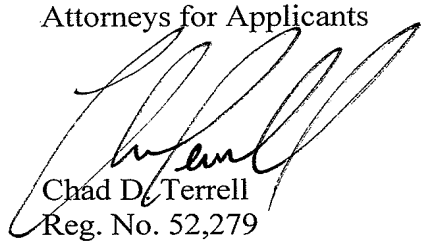
II. The Proposed Combination is Improper

Additionally, although Applicants believe the rejections have not provided an adequate explanation for the proposed *Keller1-Keller2-Replacement Instructions* combination, to avoid burdening the record and in view of the clear allowability of the claims for the reasons discussed above, Applicants do not address this issue in this submission.

Conclusion

For at least these reasons, the rejections contain clear legal and factual deficiencies, and Applicant requests allowance of all pending claims. The Commissioner is authorized to charge the $540.00 Notice-of-Appeal fee to Deposit Account No. 02-0384 of Baker Botts L.L.P. The Commissioner is authorized to charge any other necessary fees and credit any overpayments to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,
BAKER BOTTS L.L.P.
Attorneys for Applicants



Chad D. Terrell
Reg. No. 52,279

Date: February 14, 2011
Correspondence Address:
Customer No.: **45507**